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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/086,214	02/27/2002	Laung-Terng Wang	3175-Z	7756

7590 01/27/2005

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EXAMINER	
KERVEROS, JAMES C	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 01/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/086,214	WANG ET AL.	
	Examiner	Art Unit	
	JAMES C KERVEROS	2133	

-- The MAILING DATE of this communication appears on the cov r sheet with th corr spond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-80 and 84* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15 and 52-55* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/14, 25/ 02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election with traverse of Group I, species A (claims 1-15, 52-55) in the reply filed on October 21, 2004 is acknowledged. The traversal is on the ground(s) that a new claim 84 has been added and is linking to Group I and Group II claims as well as being generic to the species of Groups A, B, C and D of the elected Group I, since new claim 84 is effect a linking claim requiring examination of all claims, applicant traverses the restriction requirement as between the claims in Group I (claims 1-69) and Group II (claims 70-80).

The Examiner does not find Applicant's argument to be persuasive, because the newly submitted claim 84 is directed to an invention that is independent or distinct from the invention originally claimed. Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 16-51, 56-80 and 84 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

The requirement is still deemed proper and is therefore made FINAL.

Claims 81, 82 and 83 have been cancelled

Claims 1-80 and 84 remain pending in the application. Claims 1-15 and 52-55 are presently under examination.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 52, 53, 55 are rejected under 35 U.S.C. 102(e) as being anticipated by Kim (U.S. Patent No. 6,122,762) ISSUED: September 19, 2000, FILED: September 15, 1998.

Regarding Claim 52, Kim discloses a method for diagnosing scan cores (310), having an embedded DFD (design-for-debug) circuitry in a memory interface device (40), the DFD circuitry comprising a debug controller 400 and a JTAG TAP circuit 100, Figure 3, which is a state diagram of the TAP controller 10 of Figure 1. The TAP controller 10, driven by the TCK input, responds to the TMS input as shown, the method comprising the steps of:

(a) Issuing a DBG SCAN command (DRAM_debug) generated as a result of the test/debug instruction form register 210 to control the debug controller 400 and a JTAG TAP circuit 100 in the scan cores.

(b) Issuing a SELECT command (SELECT_DR_SCAN) for shifting in selected scan cores for diagnosing the scan cores by the debug controller 400 and a JTAG TAP circuit 100.

(c) Issuing a first SHIFT command (SHIFT_DR) for shifting in a predetermined scans pattern (TDI) to scan cells within selected scan chains for diagnosis.

(d) Issuing one or more CAPTURE (CAPTURE_DR) commands for capturing output responses into the scan cells.

(e) Issuing a second SHIFT command (SHIFT_IR) for shifting a new predetermined scan pattern (TDI) into and out of the scan cells within the selected scan chains (boundary-scan chain 332).

(f) Repeating steps of (d)-(e) by capturing and shifting the data out of the (boundary-scan chain 332) until scan diagnosis is done.

(g) Issuing a STOP command (PAUSE_DR) for generating a stop control signal to stop the scan operation.

Regarding Claim 53, Kim discloses providing a central DFD controller (400) for accepting the commands and generating the scan debug mode (DRAM_debug) and the stop control signal (PAUSE_DR) to control the debug controller 400 and a JTAG TAP circuit 100.

The DFD controller 400 interfaces with the DFD circuitry and a JTAG TAP circuit 100 in the integrated circuit 40, and wherein the TAP controller 100 is constructed according to a selected Boundary-scan Standard, Figure 4.

Regarding Claim 55, Kim discloses the commands are further used in a DFD circuitry in a memory interface device (40) comprising a debug controller 400 and a JTAG TAP circuit 100, for diagnosing scan cores (310), Figure 4.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 54 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim (U.S. Patent No. 6122762).

Regarding Claim 54, Kim substantially discloses the claimed invention as applied to independent claim 52, above. Kim does not explicitly enumerate the different faults for associated with the scan cores. It is well known in the art, that the purpose of incorporating a DFD circuitry in an integrated circuit, IC, is to diagnose failures under various fault conditions. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to incorporate various fault conditions, as it is well known in the art, in the apparatus of Kim, so as to evaluate the proper operation of scan cores of an integrated circuit, IC.

Claims 1-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim (U.S. Patent No. 6122762).

Regarding independent Claim 1, Kim substantially discloses an apparatus for inserting a DFD circuitry in a memory interface device (40), the DFD circuitry comprising a debug controller 400 and a JTAG TAP circuit 100, for diagnosing scan cores (310), the apparatus comprising:

(a) A DFD selector (output multiplexer BO1-16) corresponding to the output cells DCB1-16 of the data boundary-scan register 332, for selecting (F_core_data 0-15) from scan cores (310), for simultaneously diagnosing the core data, Figure 6.

(b) A scan connector (pins MPIN_data 0-15) for connecting multiple scan chains of the data boundary-scan register 332 to the scan cores 310 through the input cells DCA1-16, Figure 6.

(c) A scan clock generator in the TAP controller 100 for providing clock signal (Clockdr) or the debug control logic 410 for providing clock signal (Cap_clk) for clocking the capture flip-flop AC 1-16 of each input cell DCA1-16, Figure 6.

Kim does not explicitly disclose a multiplexer for connecting the DFD selector and the scan connector to a TAP (test access port) controller in the integrated circuit. However, Kim discloses a boundary-scan register 330, which is part of 300 coupled to the TAP controller 100, Figure 4. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use boundary-scan register, as taught by Kim, for the purpose of communicating a TAP (test access port) controller. A person skilled in the art would have been motivated to couple a TAP (test

access port) controller with a boundary-scan register, since the TAP controller is in compliance with IEEE STD 1149.1, thus avoiding the need of additional discrete components.

`Regarding Claim 2, Kim discloses a scan debug mode (DRAM_debug) generated as a result of the test/debug instruction form register 210, wherein the scan debug mode is set to logic value 1 (ACTIVE) when the scan cores are to be diagnosed, and set to logic value 0 (INACTIVE) when the scan cores are not to be diagnosed, accordingly: "When the signal DRAM_debug becomes active and the signal Debug_write becomes inactive, a data signal output from the DRAM device 80 is loaded into a corresponding capture flip-flop ACi".

Regarding Claim 3, Kim discloses the scan debug mode is generated by a central DFD controller (debug controller 400), which interfaces with said TAP controller 100, and the DFD circuitry (debug control logic 410). The TAP controller 100 is constructed according to a selected Boundary-scan Standard IEEE STD 1149.1, which includes a test access port (TAP) comprising TDI (test data in), TDO (test data out), TCK (test clock), TMS (test mode select), and selectively TRSTB (test reset) such as an optional input, a test reset TRSTN, although not shown, Figure 4.

Regarding Claims 4, 12, 13, Kim does not explicitly enumerate the different faults for associated with the scan cores. It is well known in the art, that the purpose of incorporating a DFD circuitry in an integrated circuit, IC, is to diagnose failures under various fault conditions. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to incorporate various fault conditions, as it

is well known in the art, in the apparatus of Kim, so as to evaluate the proper operation of scan cores of an integrated circuit, IC.

Regarding Claim 5, Kim discloses the DFD selector (output multiplexer BO1-16) corresponding to the output cells DCB1-16 of the data boundary-scan register 332, which comprises a shift register of 2 or more bits for each scan core (310), wherein the shift register 332 is controlled by the TCK and its scan data input (Sin) and scan data output (Sout) are connected to the TDI and the TDO via a multiplexer (BO1-16).

Regarding Claim 6, Kim discloses the scan connector (pins MPIN_data 0-15) further comprising a plurality of multiplexer (BO1-16) coupled with the DRAM data bus pins MPIN_data 0-15 via tri-state buffers (BF1-16) to stitch the multiple scan chains together as one serial scan chain (boundary-scan register 332) and connect its scan data input and scan data output to said TDI and said TDO, respectively. The multiplexer are controlled by said scan debug mode (DRAM_debug).

Regarding Claim 7, Kim discloses the scan connector (pins MPIN_data 0-15) further comprising a plurality of multiplexer BO1-16) to stitch the multiple scan chains together as one serial scan chain (boundary-scan register 332) and insert the serial scan chain before or after the boundary- scan chain 332, wherein the multiplexer are controlled by the scan debug mode (DRAM_debug).

Regarding Claim 8, scan connector (pins MPIN_data 0-15) further comprising a plurality of multiplexer BO1-16) to stitch the multiple scan chains together as one serial scan chain (boundary-scan register 332) and insert the serial scan chain before or after

the boundary- scan chain 332, wherein the multiplexer are controlled by the scan debug mode (DRAM_debug).

Regarding Claim 9, Kim discloses the scan connector (pins MPIN_data 0-15) further comprising a lock-up element (A01) D flip-flop between DCA1 and DCB1 scan cells to form a serial scan chain (boundary-scan register 332).

Regarding Claim 10, Kim discloses the scan clock generator in the TAP controller 100 for providing clock signal (Clockdr) or the debug control logic 410 for providing clock signal (Cap_clk) for clocking the capture flip-flop AC 1-16 of each input cell DCA1-16, Figure 6, further comprising a clock phase generator and a scan clock controller part of TAP controller.

Regarding Claim 11, Kim discloses the clock phase generator is controlled by the test clock signal TCK, which is input to TAP controller 100, and generates a plurality of non-overlapping clocks, as inputs shown in Figure 5. The controller connects the capture clocks including the TCK, and the non-overlapping TCK clocks. The TCK input is independent of the system clocks for the chip so that test operations can be synchronized between different chips.

Regarding Claim 14, Kim discloses the state diagram of the TAP controller 10 of FIG. 1, driven by the TCK input, responding to the TMS input as shown in Figure 3, where the TAP controller generates signals, including Shift DR, Capture DR, and Update DR, according to the Boundary-scan Standard.

Regarding Claim 15, Kim discloses the DFD circuitry in a memory interface device (40) including a debug controller 400 and a JTAG TAP circuit 100, for diagnosing scan cores (310), Figure 4.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Rutkowski (U.S. Patent No: 5,623,503), Method and apparatus for partial-scan testing of a device using its boundary-scan port, DATE-ISSUED: April 22, 1997.

Rutkowski discloses Partial-Scan testing of an integrated circuit (10) having a Boundary-Scan architecture (18) accomplished by a Partial-Scan controller (36), including the claimed limitations of scan clock generator (46) which operates to clock each of the scan flip-flops 17 in accordance with one of a set of system clock signals. A scan connector (input/output connection 21) for linking each Boundary-Scan cell 20 in the chain with the core logic 12 of the integrated circuit 10, Figure 1. Rutkowski does not explicitly disclose a DFD controller.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

U.S. PATENT OFFICE
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Date: 12 January 2005
Office Action: Non-Final Rejection

By: _____

JAMES C KERVEROS
Examiner
Art Unit 2133

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